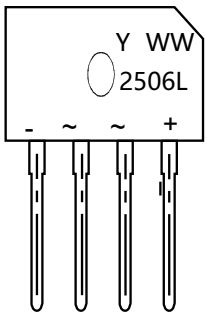
Low VF Bridge Rectifiers



PIN	DESCRIPTION
1	Input Pin ~
2	Input Pin ~
3	Output Anode +
4	Output Cathode -

Features

- Glass Passivated Chip Junction
- Low I_{RRM}
- Low V_F
- High V_{RRM}

Benefits

- Case: GBU
- Terminals: Solderable Per MIL-STD-750
- Reduced power loss and switching transistor
- Reduced snubbing

Ratings at 25 °C ambient temperature unless otherwise specified.
Single phase half-wave 60 Hz, resistive or inductive load, for capacitive load current derate by 20 %.

	Symbols		
Maximum Repetitive Peak Reverse Voltage	V_{RRM}	600	V
Maximum RMS voltage	V_{RMS}	420	V
Maximum DC Blocking Voltage	V_{DC}	600	V
Average Rectified Output Current	I_o	25	A
Peak Forward Surge Current 8.3 ms Single Half Sine Wave Superimposed on Rated Load (JEDEC Method)	I_{FSM}	300	A
Maximum Forward Voltage at 12.5 A	V_F	0.95	V
Maximum DC Reverse Current @TA=25 °C at Rated DC Blocking Voltage @TA=125 °C	I_R	10 500	μA
Typical Junction Capacitance Note1	C_j		pF
Operating and Storage Temperature Range	T_j, T_{stg}	-55 ~ +150	°C

Note: 1. Measured at 1MHz and applied reverse voltage of 4 VDC.
2.Mounted on glass epoxy PC board with 4×1.5 æ1.5 （3.81×3.81 cm）copper pad

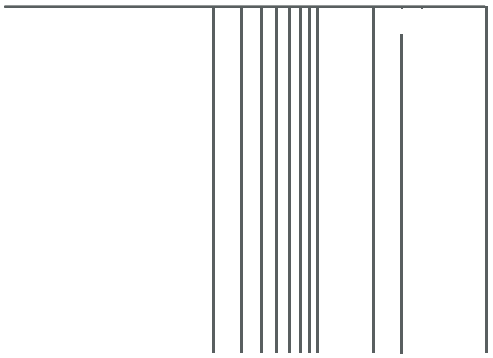
RATINGS AND CHARACTERISTICS CURVES (TA = 25 ˚C unless otherwise noted)

If, Average Forward Current (A)

75 100

Tc, Case Temp (°C)

Current Derating, Case

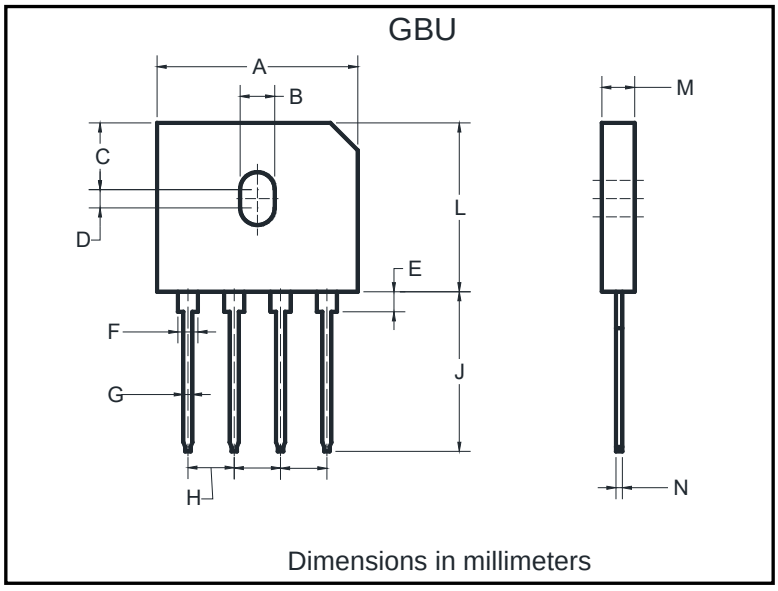


Typical Junction Capacitance

50

VR, Reverse Voltage (Volts)

Typical Reverse Current



Dim	Min	Max
A	21.70	22.50
B	3.40	4.10
C	7.40	8.00
D	1.65	2.26
E	2.25	2.85
F	2.05	2.4
G	1.02	1.37
H	4.83	5.43
J	17.0	18.6
L	18.3	18.9
M	3.30	3.66
N	0.46	0.66